

----- BEGINNING OF RESUME -----

ALI DASDAN

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++ OBJECTIVE

Leadership (technical or managerial) position where my many years of leadership and research and development experience will benefit the team and the company.

++ SUMMARY

Successfully worked in many roles (architect, tech lead, manager, researcher, engineer, mentor, coder, project manager, process manager). Led a sophisticated software product from conception to its first-time release (currently the market leader used by top chip companies). Represented the company for international and domestic customers as well as in many conferences. Currently working in a leadership role at Yahoo! Web Search, reporting directly to the VP of Web Search. Very strong and quick in generating innovative ideas in different areas. Highly motivated and enthusiastic driver. Very good mentor (from peer reviews and performance of those mentored). Produced innovative and production solutions on many challenging problems in different areas.

++ RESEARCH AND DEVELOPMENT EXPERIENCE

+ 2006-present Director, Web Search, Yahoo! Inc., Santa Clara, CA, USA

o Built and managing a talented team of engineers. Our focus is white-box metrics and monitoring, data / system analysis and debugging, algorithm / system development, and innovation in search and other areas. We analyze web search systems (crawlers, web graphs, indexers, search and proxy tiers, etc), web search data (discovered and crawled content, hierarchical web graphs, indexed content, system logs, user click / view / visit logs, etc) and the trends on the web (static vs dynamic content trends, sitemaps / robots.txt usage, user tags, etc). We end up using techniques from distributed systems on the grid (via Hadoop and Pig), data mining, machine learning, web search technology, performance analysis, metrics, statistics, and more. We create automated monitoring and debugging infrastructure for web search pipeline. We implement and monitor the metrics we design. We deployed the first production system on Hadoop in the summer of 2006, which was for analyzing crawler logs for problems.

+ 2002-2005 Senior Staff R&D Engineer, PrimeTime
Static Timing Analysis (STA), Synopsys, Inc., Mountain View, CA, USA

o PrimeTime is a market leading STA sign-off tool [www.synopsys.com/products/products.html]. "Sign-off" means a customer will not send a chip for fabrication unless the chip passes PrimeTime's checks. PrimeTime is a very large software (millions of lines of C code) and maintained by a large group. It has two major

releases per year. All my implementations (mentioned below) are in PrimeTime and have been used by many customers.

- o (Statistical STA) Led a team for the research, architecture, and implementation of the Statistical STA product in Synopsys. Wrote most of the code. Represented Synopsys at (inter)national customer sites. Led a team for initial research and feasibility of the product idea. Released the product as PrimeTime VX (currently the market-leading statistical STA solution at top chip companies).

- o (Variation-aware library) Proposed and implemented a general and scalable solution to modeling process variations in cell timing libraries and characterizing such libraries (in Perl). This proposal is one of the two fundamental requirements for statistical STA.

- o (Variation-aware parasitics) Proposed a solution to parameterize parasitics. It will be implemented in the market leading parasitics extraction tool Star-RCXT of Synopsys. Using parameterized parasitics, proposed a solution for the metal mismatch problem (a tough problem that has caused some chip failures). Also using it, proposed and will implement a solution to enable statistical STA. This proposal is one of the two fundamental requirements for statistical STA.

- o (Advanced on-chip variation) Proposed and implemented a solution to improve on-chip variation analysis with location and dependence information.

- o (Interdependent setup/hold times) Proposed and will implement the first solution in a STA tool. The solution is a very effective and simple way of eliminating optimism and reducing pessimism in STA.

- o (Inverted temperature dependence) Initiated the research of and proposed algorithms for the inverted temperature dependence and its impact in STA. This dependence is very important for some of our customers but not well-known in the digital community. Will implement the algorithms as the first solution in a STA tool.

- o (Cyclic graphs and circuits) Developed, implemented, and published an algorithm for the problem of computing longest simple paths in cyclic combinational tools (an NP-hard problem). This algorithm is the basis for the "dynamic loop breaking" mode of PrimeTime.

- o (Interacting clocks, number theory) Developed a mathematical sound solution for computing the least common multiple of floating-point clock periods and expanding clock waveforms. Implemented the solution in a module that is shared by three major commercial tools of Synopsys.

- o (Timing graph propagation) Led a small team for the re-architecture and implementation of the fundamental propagation module (delay/slew calculation and binding module). Generalized the propagation from arc based to stage based. Reduced the incoming rate of bugs to almost zero.

- o (Consistency checking) Designed and implemented a highly successful infrastructure for software consistency checking (a novel concept in software engineering). It helped find 100s of bugs hidden from a very comprehensive regression test suite. It is now a mandatory requirement for all internal re-architecture and module refinement projects.

+ 1999-2002 Member of Technical Staff, Advanced Technology Group (ATG), Synopsys, Inc., Mountain View, CA, USA

- o ATG is the corporate research department of Synopsys [www.research.synopsys.com].
 - o (DFM: Design for manufacturability) Performed an in-depth study of the opportunities and produced an influential internal report.
 - o (Low power design) Proposed and implemented algorithms for synthesis with multiple supply and threshold voltages [U2].
 - o (Chip design) Designed and taped out the ATG-SI chip in a 4-person team. Synthesized five blocks from RTL to tape-out for leakage power and performance experiments (www.synopsys.com/news/announce/press2002/umc_pr.html).
 - o (SystemC: [www.systemc.org]) Designed and implemented high-performance arbitrary precision arithmetic data types (in C++, ~24K lines). Contributed to the design of the other arithmetic and logical types. Also contributed to the VSIA System-Level Design (SLD) Data Types standardization effort [www.vsi.org]. A member of a 5-person team that made the first release.
 - o (SystemC Compiler: C/C++ based behavioral and register transfer level synthesis) Designed and implemented main optimization (loop unrolling) and translation (to VHDL and Verilog) passes (in C, ~10K lines). Documented and presented the infrastructure in significant detail. A member of the team that made the first release.
 - o (Performance analysis of discrete event systems) Performed the first theoretical and experimental work on all cycle period algorithms (in C++, ~17K lines). Also proposed an improved cycle period algorithm. These algorithms are fundamental to the performance analysis of cyclic (discrete-event) systems.
 - o (Constraint satisfaction) Proposed and implemented the first strongly polynomial-time algorithm for resolving temporal and spatial difference constraint violations [S2,C17-C16]. This algorithm has fundamental applications in scheduling, constraint satisfaction, real-time and multimedia systems, and layout compaction.
 - o (Web page design) Proposed, designed, and implemented the ATG's original internal web site (in Perl, ~4K lines).
- + 1997-1999 Visiting Scholar, The Center for Embedded Computer Systems, University of California, Irvine, CA, USA
- + 1996-1999 Teaching and Research Assistant, University of Illinois at Urbana-Champaign, IL, USA
- o (PhD work: Performance analysis of embedded systems) Proposed a timing-driven hardware / software codesign methodology for the design and validation of embedded real-time systems. It enables the automatic derivation and validation of both throughput (rate) and latency constraints [T2,J3-J2,C12-C7]. Implemented it in a tool called RADHA-RATAN (in C++, ~10K lines).
 - o (Reconfigurable computer architecture) Proposed ways of using reconfigurability for efficient memory hierarchy management for the MORPH project. Implemented a cache simulator using MINT for evaluation.
- + 1997,1998 Summer Intern, Conexant, Newport Beach, CA, USA

- o (Hardware/software co-validation) Evaluated Mentor Graphics' Seamless Co-Verification Environment (Seamless CVE) for the company. Provided the key criteria for the purchase and deployment decision.

- o (PhD work: Performance analysis of embedded systems) Designed and implemented parts of RADHA-RATAN. Presented a detailed scenario in which this tool would be useful within Conexant.

+1991-1994 Teaching and Research Assistant, Bilkent University, Ankara, Turkey

- o (MS work: Graph and hypergraph partitioning) Proposed two novel algorithms and implemented them together with Simulated Annealing for multiway graph and circuit partitioning in the ALATURKA partitioning software package (in C, ~12K lines) [T1,J1,C2]. These algorithms are the first to relax locking in the famous Kernighan-Lin algorithm and its derivatives.

- o (Optimization via genetic algorithms and neural networks) Developed the first genetic synthesis of unsupervised neural network algorithms. Demonstrated the existence of improved unsupervised learning algorithms on Kohonen's Self Organizing Map.

++ EDUCATION

- o Doctor of Philosophy (PhD) 1999
Computer Science [www.cs.uiuc.edu]
University of Illinois at Urbana-Champaign, IL, USA.
Dissertation: Timing Analysis of Embedded Real-Time Systems
Advisor: Prof. Rajesh K. Gupta [www.cse.ucsd.edu/~gupta]
Comprehensive exam areas: Theory (Algorithms and Complexity), Computer Architecture, and Artificial Intelligence
Qualifying exam area: Computer Architecture
GPA: 4.00/4.00

- o Master of Science (MS) 1993
Computer Engineering and Information Science [www.cs.bilkent.edu.tr]
Bilkent University, Ankara, Turkey.
Thesis: Graph and Hypergraph (Circuit) Partitioning
Advisor: Prof. Cevdet Aykanat [www.cs.bilkent.edu.tr/~aykanat]
GPA: 3.90/4.00

- o Bachelor of Science (BS) 1991
Computer Engineering [www.cmpe.boun.edu.tr]
Bogazici University, Istanbul, Turkey.
Thesis: Course Scheduling in Prolog
Advisor: Prof. Selahattin Kuru [irdc.isikun.edu.tr/people/kuru]
GPA: 3.64/4.00
(high honors, 2nd in the dept., 7th in the engineering school)

++ PROGRAMMING EXPERIENCE

- o Expert level: Perl (2003-present: Production and prototyping work at Yahoo! and Synopsys), C (2003-2006: PrimeTime tools at Synopsys), C++ (1994-2003: SystemC library and synthesis systems at Synopsys and PhD work), C (1991-1994: Graph and circuit partitioning tools), Pascal (1987-1991: BS work).

- o Programmed on many languages and systems (including parallel computers).

++ TEACHING EXPERIENCE

o Taught many classes, presented in many conferences, gave many internal and external talks. See the details at <http://www.dasdan.net/ali/teaching.php>.

++ AWARDS

o Received innovation awards, competitive fellowships and scholarships, and an outstanding teaching assistant award. See the details at <http://www.dasdan.net/ali/awardsnhonors.php>.

++ SERVICE

o Served as conference program and organizing committee member, conference publication chair, session chair, and paper reviewer. Also served as a judge for a middle school science competition and as a mentor to interns. See the details at <http://www.dasdan.net/ali/service.php>.

++ PATENTS AND PUBLICATIONS

o Published 3 issued patents, 14 pending patents, many publications (book chapter, journal, and conference), and a tutorial in the WWW'09 conference. See the details at <http://www.dasdan.net/ali/publications.php>.

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